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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,502	01/20/2004	Terry C. Coughlin JR.	ROC920030381US1	1485

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EXAMINER	
GARBOWSKI, LEIGH M	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,502	COUGHLIN, TERRY C.	
	Examiner	Art Unit	
	Leigh Marie Garbowski	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☒ Claim(s) 2-6,8 and 9 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 20 January 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

Claims 2-6, 8-9 are objected to because of the following informalities: --mask-- should be inserted after "(LVT)" [claim 2, line 4; claim 3, line 3; claim 5, line 3; claim 8, line 3; claim 9, line 2] to clarify the feature; "PFETs" [claim 3, line 5] should be singular to clarify antecedent basis; "each" [claim 4, lines 4 and 7; claim 5, line 4; claim 6, lines 2 and 3] suggests an antecedent basis that is not apparent; and --circuit-- should be inserted after "(SVT)" {line 3] to clarify the feature. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen [U.S. Patent #6,078,195].

As per claim 4, an AVT circuit library comprising: a plurality of hybrid AVT circuits, each said hybrid AVT circuit including a PFET having a LVT [column 4, lines 6-8, 36-37, 49-50; column 5, lines 21-23; column 6, lines 23-35]; and an NFET having a SVT [column 4, lines 6-8, 37-38, 50-52; column 5, lines 21-23; column 6, lines 23-35]. As per claim 5, wherein said hybrid AVT circuits include a corresponding SVT circuit having a LVT mask added over each said SVT PFET to convert each said SVT PFET to said LVT PFET [column 11, lines 2-18]. As per claim 6, wherein said LVT PFET is provided in an Nwell region isolated from said NFET in each said hybrid AVT circuit [column 11, lines 2-18].

Claims 4-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Helm et al. [U.S. Patent #6,849,492B2].

As per claim 4, an AVT circuit library comprising: a plurality of hybrid AVT circuits, each said hybrid AVT circuit including a PFET having a LVT [column 5, lines 5-25]; and an NFET having a SVT [column 4, lines 59-62; column 5, lines 10-25]. As per claim 5, wherein said hybrid AVT circuits include a corresponding SVT circuit having a LVT mask added over each said SVT PFET to convert each said SVT PFET to said LVT PFET [column 8, lines 10-26; column 9, lines 25-49]. As per claim 6, wherein said LVT PFET is provided in an Nwell region isolated from said NFET in each said hybrid AVT circuit [column 8, lines 10-26; column 9, lines 25-49].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. [U.S. Patent #5,666,288] in view of Chen [U.S. Patent #6,078,195].

As per claims 1/7, Jones et al. teach a method/computer program product comprising the steps of: identifying circuits in a circuit library [column 1, lines 11-12; column 3, lines 29-32; column 5, lines 47-60; column 6, lines 48-57]; for each circuit, replacing each transistor to provide a hybrid circuit [column 3, lines 39-60; column 4, lines 57-61; column 5, lines 66-67; column 6, lines 37-44; column 8, lines 30-35]; and saving each said hybrid circuit in an alternate circuit library [column 3, lines 61-62; column 4, lines 57-61; column 7, lines 61-64]. However, Jones et al. do not explicitly teach SVT circuits, SVT PFETs or LVT PFETs. Chen teaches providing mixed SVT and LVT devices including PFETs [column 4, lines 6-8, 36-37, 49-50; column 5, lines 21-23; column 6, lines 23-35], and making a library [column 6, lines 33-35]. Considering that Jones et al. suggest changing each transistor to accommodate voltage characteristics [column 6, lines 36-44; column 8, lines 10-12, 30-35; column 10, lines 21-30] and that Chen suggest making a library with SVT and LVT devices including PFETs [column 6,

lines 33-35], a person of ordinary skill in the art at the time of the invention would have found it obvious to combine these teaching to obviate the claimed invention because "its merits in standby power, speed and noise margin, such mixed-low-and-regular-V_t logic books can have a wide use in VLSI designs (e.g., high performance microprocessor design)" [Abstract, lines 13-16]. As per claims 2/8, Chen further teaches wherein the step of replacing each SVT PFET with a LVT PFET includes the step of adding a LVT mask over each said SVT PFET [column 11, lines 2-18]. As per claims 3/9, Chen further teaches wherein the step of adding a LVT mask over each said SVT PFET includes the step of adding a single shape defining said LVT mask over an Nwell region to convert each said SVT PET to said LTV PFET [column 11, lines 2-18].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Friend et al. [U.S. Patent #6,668,358 B2] disclose the concepts of replacing FET devices in a library [column 2, lines 51-65; column 8, lines 17-36] and the drawbacks of using high VT FETs [column 2, lines 26-32; column 7, lines 44-46], but actually teach away from the present invention by replacing low VT blocks with high VT blocks. Burr et al. [U.S. Patent #5,780, 912] disclose providing low threshold voltage MOS devices [column 15, lines 64-65]. Briggs [U.S. Patent #4,595,845] discloses a CMOS IC comprising a standard n-channel threshold voltage and a non-standard p-channel threshold voltage [column 2, lines 18-23].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 571-272-1893 and e-mail is Leigh.Garbowski@uspto.gov. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LEIGH M. GARBOWSKI
PRIMARY EXAMINER